REMARKS

Pending Claims

Claims 164-175 are pending in this application. Claims 164-169 have been allowed. Claims 170, 173-175 have been amended. No new matter has been added.

Office Interview Summary

Applicants appreciate the granting of an Office Interview in the above-identified application on November 28, 2005. In the Interview, the Examiner and the below named attorney discussed amendments to independent claims 170, 173, 174 and 175. At the conclusion of the Interview, amendments to the claims were proposed that would be acceptable to the Examiner, subject to further consideration upon submission of a formal Reply to the outstanding Office Action. In the Reply submitted herewith, Applicants have adopted the proposed amendments discussed in the Interview, in their entirety, and hereby request reconsideration and reexamination of the application in view of the foregoing amendments and the following remarks.

35 U.S.C. §§ 102 and 103

Applicants request reconsideration of the rejection of claim 170 under 35 U.S.C. § 102(e) as being anticipated by Nishida et al, U.S. Patent 5,436,848 (Nishida) and the rejection of claims 171-175 under 35 U.S.C. § 103(a) as being unpatentable over Nishida in view of the foregoing amendments and for the following reasons.

Claim 170 is specifically directed to a fabricating method for processing and transporting a lot which is constituted of a plurality of semiconductor wafers wherein a predetermined unit time employed throughout the fabricating method is set to be longer than the shortest required time for processing the lot in each of the processing apparatuses but shorter than the longest required time for processing the lot in each of the processing apparatuses. The description of Embodiment 7 which begins on page 134 of the specification supports the processing and transporting of a lot of wafers. See Table 9 on page 138 of the specification, for example, which shows the processing time for a plurality of processes for a lot constituted of 24 wafers. See also page 137, lines 1-7 which describe the a transporting mechanism and interface connected to the processing apparatuses that handles a lot of wafers.

Claims 173-175 are each directed to a fabricating method in which a predetermined unit time common to all of the plurality of processing apparatuses and the inter-apparatus transporter is set to be longer than one minute of processing time and to be at least as long as the shortest processing time, but shorter than the longest required time for either processing in each of the processing apparatuses or transporting by the inter-apparatus transporter (claims 173 and 175) or shorter than the longest required time for processing in each of the processing apparatuses (claim 174). An example of a short processing time is one minute of processing time. See page 39, lines 4-6 of the specification for an example of a film deposition process which requires one minute of processing time.

Nishida et al., U.S. Patent No. 5,436,848 teaches processing semiconductor wafers according to a predetermined schedule in which the schedule is based on the processing time of the longest step, which is a time interval of 70 seconds. All processing and movements are

based on the time of the longest step so as to achieve synchronized processing and movement of the wafers. Therefore, Nishida only discloses using a time interval of 70 seconds but does not disclose using a unit time that is common to all of the processing apparatuses and that is longer than the shortest required time for processing one of the wafers in each of the processing apparatuses but shorter than the longest required time for processing in each of the processing apparatuses, as claimed by Applicants in claim 170. Accordingly, the 35 U.S.C. § 102(e) rejection of claim 170 should be withdrawn.

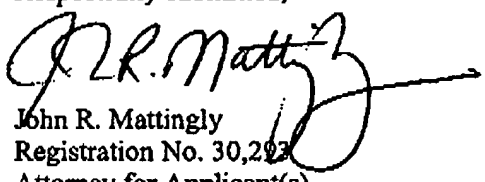
With respect to claims 171 and 172, these claims are dependent from claim 170, which is asserted to be allowable for the foregoing reasons. Accordingly, claims 171 and 172 should be allowed at least for being dependent from an allowable base claim.

The disclosure of Nishida also fails to disclose a predetermined unit time which is longer than one minute and at least as long as the shortest processing time, but shorter than the longest required time for either processing in each of the processing apparatuses or for transporting by the inter-apparatus transporter (claims 173 and 175) or for processing in each of the processing apparatuses (claim 174). Nishida neither teaches nor suggests these aspects of the claimed invention of claims 173-175. Accordingly, it is respectfully submitted that the rejection of claims 171-175 under 35 U.S.C. §103(a) as being unpatentable over Nishida should be withdrawn.

Conclusion

Applicants request examination of the pending claims in view of the foregoing remarks.

Respectfully submitted,



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